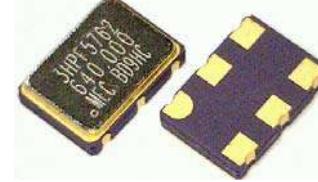


| | | | | | | | | | |
|----|---------------------|-------------------|-------------------|-----------|-----|------|------|----------------|----------------|
| HP | LVPECL Differential | F group 0.5 ps | W group 4.0 ps | Thru-Hole | SMD | 2.5V | 3.3V | Min. 750KHz | Max. 800MHz |
|----|---------------------|-------------------|-------------------|-----------|-----|------|------|----------------|----------------|

Applications

- HPF and HPW uses a high-Q fundamental crystal and a low jitter multiplier circuit.
- HPF offers a <1 ps phase jitter. "HPW" offers moderate jitter at a low cost.



General specifications , at Ta=+25°C , CL=15pF

| Model | " HPF " series | | | | " HPW " series | | | | | | | | | | | | |
|---|---|---|---------------|----------|--|---|--|--|--|--|--|--|--|--|--|--|--|
| Technology | High Q fundamental crystal + low jitter multiplier circuit | | | | High Q fundamental crystal + multiplier circuit | | | | | | | | | | | | |
| Output Logic | LVPECL Differential | | | | | | | | | | | | | | | | |
| Available Frequency Range | 38.0 MHz ~ 640.0 MHz | | | | 750 KHz ~ 800.0 MHz | | | | | | | | | | | | |
| Supply Voltage V _{DD} | +2.5 V _{DD} ± 5% | | +3.3 VDD ± 5% | | +3.3 VDD ± 5% | | | | | | | | | | | | |
| Supply Voltage Code | " 25 " | | " 3 " | | " 3 " | | | | | | | | | | | | |
| Output Logic " High " , " 1 " | V _{DD} -1.025 min. Termination: R _L =50 Ω to (V _{DD} -2.0V). See test circuit below. | | | | | | | | | | | | | | | | |
| Output Logic " Low " , " 0 " | V _{DD} -1.620 max. Termination: R _L =50 Ω to (V _{DD} -2.0V). See test circuit below. | | | | | | | | | | | | | | | | |
| Integrated Phase Jitter (12 KHz to 20 MHz) | 0.4 ps typical; 0.5 ps max. For 156.250 MHz | | | | 2.6 ps typical; 4 ps max. For 155.520 MHz | | | | | | | | | | | | |
| Period Jitter | | | | | | | | | | | | | | | | | |
| RMS ; Decoupling capacitor between V _{DD} and ground | 3 ps typical ; 5 ps max. For 156.250 MHz | | | | 4.3 ps typical. For 155.520 MHz | | | | | | | | | | | | |
| Period Jitter (peak-to-peak ; Decoupling capacitor between V _{DD} and ground) | 20 ps typical ; 30 ps max. For 156.250 MHz | | | | 27 ps typical. For 155.520 MHz | | | | | | | | | | | | |
| Current Consumption (15 pF load) | 38 MHz ~ 100 MHz: 65 mA max 100.01 MHz ~ 320 MHz: 80 mA max. 320.01 MHz ~ 640 MHz: 90 mA max.. | | | | < 24 MHz: 25 mA max 24.01 MHz ~ 96 MHz: 65 mA max. 96.01 MHz~700 MHz: 100 mA max.. | | | | | | | | | | | | |
| Rise Time / Fall Time | 0.4 ns typical , 0.55 ns max. (20%↔80% of the PECL wave form) | | | | 0.6 ns typical , 1.5 ns max. (20%↔80% of the PECL wave form) | | | | | | | | | | | | |
| Frequency Stability ⁽¹⁾ Codes | Frequency Stability over Operating Temperature Range | | ± 25 ppm | ± 50 ppm | ± 100 ppm | If non-standard , please enter the desired stability after the " C " or " I " represents . For example : " C20 " ± 20 ppm over -10°C to +70°C ; " I20 " ± 20 ppm over -40°C to +85°C | | | | | | | | | | | |
| | Commercial (-10°C to +70°C) | | A | B | C | | | | | | | | | | | | |
| | Industrial (-40°C to +85°C) | | D | E | F | | | | | | | | | | | | |
| Load | R _L =50 Ω to (V _{DD} -2.0V). See test circuit below. | | | | | | | | | | | | | | | | |
| Start-up Time | 10 m sec. (max.) | | | | | | | | | | | | | | | | |
| Duty Cycle | 50% ± 5% (measured at V _{DD} -1.3V) | | | | | | | | | | | | | | | | |
| Input Static Discharge Protection | 2 KV (min.) | | | | | | | | | | | | | | | | |
| Storage Temperature | -55°C to + 150°C | | | | | | | | | | | | | | | | |
| Aging at Ta = +25°C | ± 3 ppm max. first year ; ± 2 ppm max. per year thereafter | | | | | | | | | | | | | | | | |
| Tri - State Function. <u>5761</u> on pad No. 1 <u>5762</u> on pad No. 2 | No Connection | Differential PECL and compliantary PECL outputs . | | | | | | | | | | | | | | | |
| | Disable | Both outputs are disabled (high impedance) when the Tri-state pad taken below 0.45*Vcc referenced to ground (threshold) Oscillator is always On . Only buffer stage is disabled . Disable current : 50 uA max. (at 0.0V) , Disable time : 10 ns (max.) | | | | | | | | | | | | | | | |
| | Enable | At disabled mode , both outputs are enabled when Tri-state pad is taken above 0.45*Vcc referenced to ground (threshold) ; Enable time : 10ns + one period of the output frequency (max.) | | | | | | | | | | | | | | | |
| SSB Phase Noise [dBc / Hz (typical)] | Offset | Frequency: 156.250 MHz | | | Frequency: 155.520 MHz | | | | | | | | | | | | |
| | 10 Hz | -62 | | | -62 | | | | | | | | | | | | |
| | 100 Hz | -92 | | | -95 | | | | | | | | | | | | |
| | 1 KHz | -120 | | | -120 | | | | | | | | | | | | |
| | 10 KHz | -132 | | | -125 | | | | | | | | | | | | |
| | 100 KHz | -128 | | | -121 | | | | | | | | | | | | |
| | 1 MHz | -140 | | | -120 | | | | | | | | | | | | |
| | 10 MHz | -150 | | | -140 | | | | | | | | | | | | |

⁽¹⁾ Inclusive of 25°C tolerance, operating temperature range, ±10% input voltage variation, load change, aging shock and vibration

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